In the Claims:

1-6. (cancelled)

7. (original) An integrated circuit structure, comprising:

a gate structure formed on a body of semiconductor material;

an insulating layer formed opposite said gate structure beneath said semiconductor material;

a conducting region within said insulating layer beneath said gate structure, said conducting region having sublithographic width.

8. (original) The integrated circuit of Claim 7, wherein said conducting region contacts said semiconductor material.

9. (original) The integrated circuit of Claim 7, wherein said conducting region is formed in a trench with sidewalls.

10. (original) The integrated circuit of Claim 7, wherein said semiconductor material is silicon.

11. (original) The integrated circuit of Claim 7, wherein said conducting region is separated from said semiconductor material by a dielectric material.

12. (withdrawn) An integrated circuit structure, comprising:

a substrate with an insulating layer, said insulating layer having a trench etched therein, said trench having sidewalls formed thereon;

a conducting material filling said trench;

a body of active material formed on said insulating layer over said conducting material such that said conducting material contacts said body along a substantial portion of said body;

a gate structure formed on said body of active material.

13. (withdrawn) The integrated circuit of Claim 12, wherein electrical contact is made to said conducting material.

14. (withdrawn) The integrated circuit of Claim 12, wherein said conducting material is polysilicon.

15. (withdrawn) The integrated circuit of Claim 12, wherein said insulating layer is made of an oxide.

16. (withdrawn) The integrated circuit of Claim 12, wherein a portion of said body extends beyond said gate structure on at least one end, and wherein electrical contact is made to said portion of said body.

17. (withdrawn) An integrated circuit structure, comprising:

a substrate with an insulating layer, said insulating layer having a trench etched therein, said trench having sidewalls formed thereon;

a first conducting region filling said trench;

a second conducting region contacting said first conducting region, said second conducting region being wider than said first conducting region;

a body of active material formed on said insulating layer over said first conducting region such that said first conducting region contacts said body along a substantial portion of said body;

a gate structure formed on said body of active material.

18. (withdrawn) The integrated circuit of Claim 17, wherein electrical contact is made to said conducting material.

19. (withdrawn) The integrated circuit of Claim 17, wherein said conducting material is polysilicon.

20. (withdrawn) The integrated circuit of Claim 17, wherein said insulating layer is made of an oxide.

21. (withdrawn) The integrated circuit of Claim 17, wherein a portion of said body extends beyond said gate structure on at least one end, and wherein electrical contact is made to said portion of said body.

22. (withdrawn) A fabrication method, comprising the steps of:

providing a semiconductor material with an insulating layer thereon;

etching a trench in said insulating layer;

forming sidewalls in said trench;

forming a conducting material in said trench;

wherein said semiconductor material has a transistor formed therein; and

wherein said conducting material is aligned with the channel of said transistor.

23. (withdrawn) The method of Claim 22, wherein said conducting material also contacts a conducting interconnect structure.

22. (withdrawn) The method of Claim 22, wherein said sidewalls in said trench reduce the width of said trench to sublithographic dimension.

25. (withdrawn) The method of Claim 22, wherein said conducting material contacts said semiconductor material.

26. (withdrawn) The method of Claim 22, wherein said conducting material is separated from said semiconductor material by a dielectric material.

27. (withdrawn) A fabrication method, comprising the steps of:

providing a substrate with an insulating layer thereon;

forming a trench in said insulating layer;

forming sidewalls in said trench;

filling said trench with a conducting material;

forming a transistor over said trench.

28. (withdrawn) The method of Claim 27, wherein said trench after sidewall formation is of sublithographic width.

29. (withdrawn) The method of Claim 27, further comprising a second insulating layer between said conducting material and said transistor.